

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device is provided. A first insulating layer having a gate electrode is formed on a semiconductor substrate. A second insulating layer is formed on the first insulating layer, and the second insulating layer has bit lines covered with bit line isolation layers, buried contact plugs formed between the bit lines, and a first metal contact plug
5 connected to the semiconductor substrate through the first insulating layer. A silicon nitride layer is formed on the second insulating layer. A third insulating layer is formed on the silicon nitride layer, and the third insulating layer has a second metal contact plug connected to the first metal contact plug through the silicon nitride layer. The second insulating layer includes a first landing
10 stud connected to the gate electrode through the first insulating layer. The bit lines include a direct contact plug under one of the bit line. The first landing stud is simultaneously formed with the direct contact plug. The second insulating layer further includes a second landing stud on the first landing stud. The second landing stud is larger in surface area than the first landing stud. The first metal contact plug and the buried contact plugs are simultaneously formed with an
15 electrical conducting material. The electrical conducting material includes tungsten (W). The third insulating layer further includes a metal-insulator-metal capacitor on the buried contact plug.